



STIC Search Report

EIC 2800

STIC Database Tracking Number: 119190

TO: Monica Lewis
Location: JEF 5A30
Art Unit : 2822
Monday, April 19, 2004

Case Serial Number: 10/657069

From: Scott Herzog
Location: EIC 2800
JEF4B68
Phone: 272-2663

Scott.hertzog@uspto.gov

Search Notes

Examiner Lewis,

Attached are edited first pass search results from the patent and nonpatent databases.

Colored tags indicate abstracts especially worth your review.

If you need further searching or have questions or comments, please let me know.

Thanks,
Scott Herzog

119190

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date <u>4/19/04</u>	Serial # <u>101657,069</u>	Priority Application Date _____
Your Name <u>M. Lewis</u>	Examiner # _____	
AU <u>2899</u>	Phone <u>979-1938</u>	Room <u>5A30</u>
In what format would you like your results? Paper is the default.		
<input checked="" type="radio"/> PAPER <input type="radio"/> DISK <input type="radio"/> EMAIL		

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

05 1- 15-A13-65-NV

Where have you searched so far on this case?

Circle: USPTO DWPI EPO Abs JPO Abs IBM TDB

4-39-04 10:54 AM

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs Nonpatent Literature _____ Other _____
Secondary Refs Foreign Patents _____
Teaching Refs _____

What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 55&56
Div. 101983,316 + 091884/aa7

Problem: see paragraphs 2-6
Solution: " " 87.

Please look for the materials and/or
ranges that are utilized.

Staff Use-Only	Type of Search	Vendors
Searcher: <u>HERTZOG</u>	Structure (#) _____	STN <input checked="" type="checkbox"/>
Searcher Phone: <u>2-2663</u>	Bibliographic <input checked="" type="checkbox"/>	Dialog <input checked="" type="checkbox"/>
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation _____	Questel/Orbit _____
Date Searcher Picked Up: <u>4/16/04</u>	Fulltext _____	Lexis-Nexis _____
Date Completed: <u>4/19/04</u>	Patent Family _____	WWW/Internet _____
Searcher Prep/Rev Time: <u>230</u>	Other _____	Other _____
Online Time: <u>50</u>		

FILE 'HCAPLUS' ENTERED AT 09:14:36 ON 19 APR 2004
L1 1 S US20030054606/PN OR US6656835/PN
L2 SEL PLU=ON L1 1- RN : 2 TERMS

FILE 'REGISTRY' ENTERED AT 09:14:43 ON 19 APR 2004
L3 48439 S RH/MF OR (RH/ELS AND 1/NC)
L4 2 S L2
L5 48440 S L4 OR L3

FILE 'HCAPLUS' ENTERED AT 09:15:36 ON 19 APR 2004
L6 1 S L5 AND L1
L7 5534 S CAPACITOR ELECTRODES+NT,UF,OLD,KT/CT
L8 369 S L7 AND L5
L9 0 S L7 (L) L5
L10 369 S L8 NOT L1
L11 71 S L10 NOT P/DT
L12 0 S L5(L)CAPACITORS+NT,UF/CT
L13 738 S L5(L)CAPACITOR?
L14 48 S L11 NOT PD>20010621

FILE 'ZCAPLUS' ENTERED AT 09:27:43 ON 19 APR 2004
E ATOMIC LAYER DEPOSITION+ALL/CT
E ATOMIC LAYER EPITAXY+ALL/CT
E DEPOSITION+ALL/CT
E ATOMIC LAYER EPITAXY+NT,UF,OLD/CT

FILE 'HCAPLUS' ENTERED AT 09:30:01 ON 19 APR 2004
L15 1786 S ATOMIC LAYER EPITAXY+NT,UF,OLD/CT
L16 0 S L15(L)L5
L17 3 S L15 AND L10

FILE 'HCAPLUS' ENTERED AT 09:51:19 ON 19 APR 2004
L18 1 S L14 AND L3
L19 1 S L18 NOT L1
L20 276 S L3(L)CAPACIT?
L21 273 S L20 NOT L19 NOT L17 NOT L1 NOT L11
L22 0 S L15 AND L21
L23 QUE ABB=ON PLU=ON LAMEL? OR FILM? OR THINFILM? OR LAYER? OR
OVERLAY? OR OVERLAID? OR LAMIN? OR MULTI(W)LAYER? OR MULTILAYER?
? OR SHEET? OR LEAF? OR FOIL? OR COAT? OR TOPCOAT? OR OVERCOAT?
OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR
ENWRAP? OR OVERSPREAD? OR LINING? OR LINER# OR LINED
L24 6706 S ALD OR ALG OR ((ATOM## OR ATOMISTIC? OR
ATOMICAL?) (2A)L23) (2A) (GROW#### OR EPITAX##### OR DEPOSIT? OR
DEP## OR DEPN# OR LAYING OR LAID OR LAIN OR PUT? OR SET?)
L25 2 S L24 AND L21
L26 2 S L25 NOT L19 NOT L17 NOT L1 NOT L11
L27 2 S L26 AND P/DT
L28 43 S L24 AND (RH OR RHODIUM)
L29 38 S L28 NOT L25 NOT L19 NOT L17 NOT L1 NOT L11
L30 22 S L29 NOT P/DT NOT PD>20010621
L31 543700 S CAPACITORS+NT,UF/CT OR CAPACITOR ELECTRODES+NT,UF/CT OR CAPAC
L32 1 S L31 AND L30
L33 7 S L31 AND L29 NOT L30

File 2:INSPEC 1969-2004/Apr W2
(c) 2004 Institution of Electrical Engineers

Set	Items	Description
S1	30134	(CAPACITORS) (January 1969)
S2	3517	CI=(RH SS OR RH EL)
S3	8	S1 AND S2

L14 ANSWER 11 OF 48 HCPLUS COPYRIGHT 2004 ACS on STN
 AN 2001:100563 HCPLUS DN 134:245806
 TI New electrode-barrier structures for high density ferroelectric memories
 AU Vedula, R.; Desu, C. S.; Tirumala, S.; Bhatt, H. D.; Desu, S. B.; Lee, K. B.
 SO Applied Physics A: Materials Science & Processing (2001), 72(1), 13-20
 CODEN: APAMFC; ISSN: 0947-8396
 AB In this paper, two electrode-barrier structures based on Pt-Rh and Pt-Ir alloys and their oxides are proposed for high-d. ferroelec. memory applications. These electrode-barriers are multilayered, comprising a diffusion barrier (PtRhO_x or PtIrO_x), metal alloy (PtRh or PtIr), and another PtRhO_x or PtIrO_x layer for fatigue reduction in the case of PZT capacitors. Both lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT) capacitors based on the electrode-barriers were used in the present study. The electrode-barrier structure acts as a conducting electrode as well as an excellent diffusion barrier for lead, bismuth, oxygen and silicon. The PZT test capacitors fabricated on these electrode-barriers showed excellent fatigue resistance with other ferroelec. properties being similar to those on Pt. Also, these electrode-barriers are stable, and remain conductive even up to the processing temps. of SBT (750°C). This makes direct integration of both PZT and SBT capacitors on to a poly-Si plug attainable. In addition, the conducting electrode-barrier structures can be deposited in situ, directly over n+ polycryst. Si, thereby significantly improving the d. of the device.
 CC 76-3 (Electric Phenomena)
 IT Capacitor electrodes
 Dielectric hysteresis
 Dielectric polarization
 Diffusion barrier
 Ferroelectric capacitors
 Ferroelectric memory devices
 Ferroelectricity
 Leakage current
 Microstructure
 Reactive sputtering
 Semiconductor memory devices
 Sputtering
 (electrode-barrier structures for high d. ferroelec. memories)
 IT 7782-44-7, Oxygen, processes
 RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
 (sputtering gas; electrode-barrier structures for high d. ferroelec. memories)
 RN 7782-44-7 HCPLUS
 CN Oxygen (8CI, 9CI) (CA INDEX NAME)

L17 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 2004:18860 HCAPLUS
 TI Method of growing electrically conductive thin films for electronics applications
 IN Kostamo, Juhana; Soininen, Pekka J.; Elers, Kai-Erik; Haukka, Suvi
 PA Finland

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004005753	A1	20040108	US 2003-394430	20030320
	US 2002004293	A1	20020110	US 2001-858820	20010515
	US 6482740	B2	20021119		
	US 2003096468	A1	20030522	US 2002-300169	20021119

PRAI FI 2000-1163 20000515
 US 2001-858820 20010515
 US 2002-300169 20021119

AB The invention relates to a method of growing elec. conductive thin films for electronics applications, such that the film has improved step coverage and adhesion properties. A method includes depositing a metal oxide thin film on a substrate by an atomic layer deposition (ALD) process. The method further includes at least partially reducing the metal oxide thin film by exposing the metal oxide thin film to a reducing agent, thereby forming a seed layer. The reducing agent comprises one or more organic compds. that contain at least one functional group selected from a hydroxyl group, an aldehyde group, and a carboxy group.

IC ICM H01L021-8238
 NCL 438222000

IT Capacitor electrodes
 Diffusion barrier
 (method of growing elec. conductive thin films for electronics applications)

IT Atomic layer epitaxy
 (oxide film formed by; method of growing elec. conductive thin films for electronics applications)

IT 7782-44-7, Oxygen, processes 10028-15-6, Ozone, processes
 RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (epitaxy oxidant; method of growing elec. conductive thin films for electronics applications)

IT 1301-96-8, Silver oxide (AgO) 1303-58-8, Gold oxide (Au2O3) 1307-96-6, Cobalt oxide (CoO), uses 1308-06-1, Cobalt oxide (Co3O4) 1313-99-1, Nickel oxide (NiO), uses 1314-08-5, Palladium oxide (PdO) 1314-15-4, Platinum oxide (PtO2) 1314-28-9, Rhenium oxide (ReO3) 1317-38-0, Cupric oxide, uses 1317-39-1, Cuprous oxide, uses 12030-49-8, Iridium oxide (IrO2) 12036-02-1, Osmium oxide (OsO2) 12036-09-8, Rhenium oxide (ReO2) 12036-10-1, Ruthenium oxide (RuO2) 12036-35-0, Rhodium oxide (Rh2O3) 12137-27-8, Rhodium oxide (RhO2) 12165-05-8, Rhenium oxide (Re2O5) 20667-12-3, Silver oxide (Ag2O)
 RL: TEM (Technical or engineered material use); USES (Uses)
 (method of growing elec. conductive thin films for electronics applications)

L17 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 2002:674490 HCAPLUS
 TI Process for the formation of RuSixOy-containing barrier layers for high-k dielectrics
 IN Marsh, Eugene P.
 PI PATENT NO. KIND DATE APPLICATION NO. DATE
 US 2002121697 A1 20020905 US 2002-136771 20020430
 US 2002187632 A1 20021212 US 2002-215991 20020809
 US 2002190276 A1 20021219 US 2002-215990 20020809
 PRAI US 2000-651620 200000830
 AB The present invention pertains to diffusion barrier layers for semiconductor devices. The method for use in the fabrication of integrated circuits includes providing a substrate assembly having a surface. A diffusion barrier layer is formed over at least a portion of the surface. The diffusion barrier layer is formed of RuSixOy, where x and y are in the range of .apprx.0.01 to .apprx.10. The barrier layer may be formed by depositing RuSixOy by CVD, atomic layer deposition, or phys. vapor deposition or the barrier layer may be formed by forming a layer of Ru or Ru oxide over a Si-containing region and performing an anneal to form RuSixOy from the layer of Ru and Si from the adjacent Si-containing region. Capacitor electrodes, interconnects or other structures may be formed with such a diffusion barrier layer. Semiconductor structures and devices can be formed to include diffusion barrier layers formed of RuSixOy.
 IC ICM H01L023-48
 NCL 257751000
 IT Annealing
 Atomic layer epitaxy
 Capacitor electrodes
 Diffusion barrier
 Electric contacts
 Integrated circuits
 Interconnections, electric
 Semiconductor device fabrication
 (process for formation of RuSixOy-containing barrier layers for high-k dielecs.)
 IT 7439-88-5, Iridium, uses 7440-04-2, Osmium, uses 7440-05-3, Palladium, uses 7440-06-4, Platinum, uses 7440-16-6, Rhodium, uses 7440-18-8, Ruthenium, uses 7440-33-7, Tungsten, uses 12030-49-8, Iridium oxide (IrO₂) 12033-62-4, Tantalum nitride (Ta_N) 12036-02-1, Osmium oxide (OsO₂) 12036-10-1, Ruthenium oxide (RuO₂) 12058-38-7, Tungsten nitride (WN) 12137-27-8, Rhodium oxide (RhO₂) 18868-43-4, Molybdenum oxide (MoO₂) 187749-47-9, Ruthenium silicon oxide RL: DEV (Device component use); USES (Uses)
 (process for formation of RuSixOy-containing barrier layers for high-k dielecs.)

L19 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:384347 HCAPLUS
TI Retardation of O diffusion through polycrystalline Pt by Be doping
AU Stumpf, Roland; Liu, Chun-Li; Tracy, Clarence
SO Physical Review B: Condensed Matter and Materials Physics (1999), 59(24),
16047-16052
CODEN: PRBMDO; ISSN: 0163-1829
PB American Physical Society
AB A serious problem preventing the use of high dielec. oxide materials (e.g., Ba-Sr-titanate) for capacitors as part of future dynamic random access memory is the oxidation of or the O diffusion through the electrodes. Pt electrodes do not oxidize, but they allow for rapid O diffusion through the Pt film while the dielec. is deposited and annealed. This causes unwanted oxidation below the Pt film. Using 1st-principles electronic structure calcns., the authors 1st determine the O diffusion mechanism in polycryst. Pt. O diffuses as interstitial O along the grain boundary (GB) that the authors study. The calculated barrier is compatible with the exptl. estimate. The authors screen nine elements for their potential to retard O diffusion if added to the Pt in small amts. Be is the most promising candidate. Be segregates to Pt GB's at interstitial and substitutional sites. As GB interstitial Be diffuses at a rate comparable to that of O and it repels O and this leads to a stuffing of the GB. As substitutionally absorbed Be, Be has a high diffusion barrier, and it forms strong bonds to O and thus O is trapped in the GB. Preliminary exptl. results confirm the authors' theor. predictions.
IT Capacitor electrodes
IT 7439-88-5, Iridium, uses 7439-95-4, Magnesium, uses 7440-16-6,
Rhodium, uses 7440-25-7, Tantalum, uses 7440-32-6, Titanium, uses
7440-42-8, Boron, uses 7440-50-8, Copper, uses 7440-62-2, Vanadium,
uses
RL: MOA (Modifier or additive use); USES (Uses)
(retardation of oxygen diffusion through polycryst. platinum capacitor electrodes by doping)

L27 ANSWER 1 OF 2 HCPLUS COPYRIGHT 2004 ACS on STN
 AN 2004:182442 HCPLUS DN 140:227401
 TI Platinum stuffed with silicon oxide as a diffusion oxygen barrier for semiconductor devices
 IN Marsh, Eugene P.
 PA Micron Technologies, Inc., USA
 IC ICM H01L021-20
 NCL 438396000
 CC 76-3 (Electric Phenomena)
 PI PATENT NO. KIND DATE APPLICATION NO. DATE
 US 2004043578 A1 20040304 US 2002-230605 20020829 X FYI
 US 2002-230605 20020829

AB The present invention provides techniques to fabricate high dielec. MIM storage cell capacitors for dense memory cell arrays. In 1 embodiment, this is accomplished by forming a Si contact is then formed to elec. connect the formed bottom electrode layer in the container with the ≥1 associated transistor device. A Ti nitride barrier layer is then formed over the Si contact. An O barrier layer including Pt stuffed with Si oxide is then formed over the Ti nitride layer and below the bottom electrode layer. A bottom electrode layer is then formed using Pt over interior surfaces of a container formed relative to at least 1 associated transistor device on a Si substrate. Further, a high dielec. insulator layer is formed over the bottom electrode layer. A top electrode layer is then formed over the high dielec. insulator layer.

IT Vapor deposition process
 (chemical, atomic layer; platinum stuffed with silicon oxide as a diffusion oxygen barrier for semiconductor devices)

IT Diffusion barrier
 (oxygen; platinum stuffed with silicon oxide as a diffusion oxygen barrier for semiconductor devices)

IT Vapor deposition process
 (phys.; platinum stuffed with silicon oxide as a diffusion oxygen barrier for semiconductor devices)

IT Annealing
 Capacitor electrodes
 MIM capacitors
 Semiconductor device fabrication
 Semiconductor memory devices

IT 7439-88-5, Iridium, uses 7440-06-4, Platinum, uses 7440-16-6, Rhodium, uses RL: DEV (Device component use); USES (Uses)
 (capacitor electrode; platinum stuffed with silicon oxide as a diffusion oxygen barrier for semiconductor devices)

L27 ANSWER 2 OF 2 HCPLUS COPYRIGHT 2004 ACS on STN
 AN 2004:162402 HCPLUS DN 140:227207
 TI Enhanced **atomic layer deposition**
 IN Meng, Shuang; Derderian, Garo J.; Sandhu, Gurtej Singh
 PA USA
 IC ICM H01L021-44
 NCL 438656000
 CC 76-3 (Electric Phenomena)
 Section cross-reference(s): 75
 PATENT NO. KIND DATE APPLICATION NO. DATE
 PI US 2004038525 A1 20040226 US 2002-229338 20020826 X FY /
 US 2002-229338 20020826
 AB A method of enhanced **atomic layer deposition** is described. In an embodiment, the enhancement is the use of plasma. Plasma begins prior to flowing a 2nd precursor into the chamber. The 2nd precursor reacts with a prior precursor to deposit a layer on the substrate. In an embodiment, the layer includes at least one element from each of the 1st and 2nd precursors. In an embodiment, the layer is TaN. In an embodiment, the precursors are TaF5 and NH3. In an embodiment, the plasma begins during the purge gas flow between the pulse of 1st precursor and the pulse of 2nd precursor. In an embodiment, the enhancement is thermal energy. In an embodiment, the thermal energy is greater than generally accepted for ALD (>300°). The enhancement assists the reaction of the precursors to deposit a layer on a substrate.
 ST **atomic layer deposition**
 IT Vapor deposition process
 (**atomic layer deposition**; enhanced
 atomic layer deposition for forming barrier
 layer in integrated circuit device)
 IT Process control
 (computerized; of enhanced **atomic layer**
 deposition)
 IT Integrated circuits
 (enhanced **atomic layer deposition** for
 forming barrier layer in integrated circuit device)
 IT Memory devices
 (having dielec. layer between two electrodes and **atomic**
 layer deposited TaN barrier layer)
 IT Capacitors
 (integrated circuit; integrated circuit capacitors having dielec. layer
 between two electrodes and **atomic layer**
 deposited TaN barrier layer)
 IT 7440-06-4, Platinum, uses 7440-16-6, Rhodium, uses ;
 RL: DEV (Device component use); USES (Uses)
 (electrodes; integrated circuit **capacitors** having dielec.
 layer between two electrodes and **atomic layer**
 deposited TaN barrier layer)
 IT 12033-62-4, Tantalum nitride (TaN)
 RL: DEV (Device component use); FMU (Formation, unclassified); PEP
 (Physical, engineering or chemical process); PYP (Physical process); FORM
 (Formation, nonpreparative); PROC (Process); USES (Uses)
 (films; enhanced **atomic layer**
 deposition for forming barrier layer in integrated circuit
 device)

L33 ANSWER 1 OF 7 HCPLUS COPYRIGHT 2004 ACS on STN
 AN 2004:182108 HCPLUS Full-textDN 140:227341
 TI Metal plating using seed film in semiconductor applications
 IN Marsh, Eugene P.
 PA Micron Technology, Inc., USA
 PATENT NO. KIND DATE APPLICATION NO. DATE
 PI US 2004041194 A1 20040304 US 2002-231435 20020829X
 AB There is a need in the semiconductor art for creating uniform seed films for use in electroplating processes and the present invention is directed to an electroplating method for use in fabricating an integrated circuit, a method for plating, a method for use in fabricating a **capacitor**, a seed film for use in electroplating a conductive layer, and a **capacitor** for an integrated circuit. A seed film and methods incorporating the seed film in semiconductor applications is provided. The seed film includes one or more noble metal layers, where each layer of the one or more noble metal layers is no greater than a monolayer. The seed film also includes either one or more conductive metal oxide layers or one or more Si oxide layers, where either layer is no greater than a monolayer. The seed film can be used in plating, including electroplating, conductive layers, over at least a portion of the seed film. Conductive layers formed with the seed film can be used in fabricating an integrated circuit, including fabricating **capacitor** structures in the integrated circuit.
 IC ICM H01L021-20
 NCL 257306000; 438396000
 CC 76-3 (Electric Phenomena)
 Section cross-reference(s): 48, 72
 IT Vapor deposition process
 (chemical, **atomic-layer deposition**; metal
 plating using seed film in semiconductor device fabrication)
 IT **Capacitors**
 Electrodeposition
 Integrated circuits
 Oxidation
 Semiconductor device fabrication
 (metal plating using seed film in semiconductor device fabrication)
 IT 1590-87-0, Silicon hydride (Si₂H₆) 12192-97-1, Dicarbonyl(*n*5-cyclopentadienyl)**rhodium** 52438-26-3
 RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (metal plating using seed film in semiconductor device fabrication)
 IT 7439-88-5P, Iridium, processes 7440-16-6P, **Rhodium**, processes
 7440-18-8P, Ruthenium, processes 11107-71-4P 11113-84-1P, Ruthenium oxide 12645-46-4P, Iridium oxide
 RL: PEP (Physical, engineering or chemical process); PYP (Physical process); SPN (Synthetic preparation); TEM (Technical or engineered material use); PREP (Preparation); PROC (Process); USES (Uses)
 (metal plating using seed film in semiconductor device fabrication)
 IT 7631-86-9P, Silicon diOxide, processes 12680-36-3P, **Rhodium** oxide
 RL: PEP (Physical, engineering or chemical process); PYP (Physical process); SPN (Synthetic preparation); TEM (Technical or engineered material use); PREP (Preparation); PROC (Process); USES (Uses)
 (platinum doped; metal plating using seed film in semiconductor device fabrication)

L33 ANSWER 2 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 2004:80414 HCAPLUS Full-textDN 140:137734
 TI **Atomic layer deposition** of high k dielectric films
 IN Lee, Sang-in; Senzaki, Yoshihide
 PA ASML US, Inc., USA
 PATENT NO. KIND DATE APPLICATION NO. DATE
 PI WO 2004008827 A2 20040129 WO 2003-US22712 20030721
 PRAI US 2002-PV396723 20020719
 US 2002-PV396745 20020719 X

AB The present invention relates to a process to form high dielec. constant gate and **capacitor** insulators using **atomic layer deposition** and a removal processes. The method of processing a semiconductor substrate includes reacting in a reactor a 1st reactant gas, evacuating the 1st reactant gas from the reactor, reacting a 2nd reactant gas, and evacuating the 2nd reactant gas. The reacting of the 1st reactant gas reacts the 1st reactant gas with an exposed surface of the semiconductor substrate in a reactor to convert the exposed surface into a solid mono-layer. The reacting of the 2nd reactant gas reacts the 2nd reactant gas with the solid mono-layer in the reactor to convert the solid mono-layer into a gaseous compound. The evacuating of the 2nd reactant gas also evacuates the gaseous compound from the reactor.

IT Dielectric films
 Diffusion barrier
 Nitriding
 (**atomic layer deposition** of high k dielec. films)
 IT Vapor deposition process
 (chemical, **atomic layer**
deposition of high k dielec. films)
 IT Water vapor
 (vapor deposition process gas; **atomic layer**
deposition of high k dielec. films)
 IT 1306-38-3P, Ceria, uses 1314-23-4P, Zirconia, uses 1314-61-0P, Tantala
 1344-28-1P, Alumina, uses 12055-23-1P, Hafnium oxide (HfO₂)
 13463-67-7P, Titania, uses
 RL: PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
 (**dielec. film; atomic layer**
deposition of high k dielec. films)
 IT 11113-84-1P, Ruthenium oxide 12033-62-4P, Tantalum nitride (Ta_N)
 12058-38-7P, Tungsten nitride (WN) 12645-46-4P, Iridium oxide
 12680-36-3P, **Rhodium** oxide 20816-12-0P, Osmium oxide
 25583-20-4P, Titanium nitride (Ti_N) 53322-74-0P, Aluminum tantalum
 nitride 113151-72-7P, Aluminum titanium nitride 118408-58-5P, Tungsten
 nitride silicide (W(N,Si)) 209414-19-7P, Aluminum tungsten nitride
 209530-51-8P, Titanium nitride silicide (TiNSi) 403852-89-1P, Tantalum
 nitride silicide (TaNSi)
 RL: PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
 (**diffusion barrier; atomic layer deposition**
 of high k dielec. films)

L33 ANSWER 3 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 2003:1007432 HCAPLUS Full-textDN 140:51616
 TI Process for direct **deposition** of atomic layer deposited RhO₂
 IN Marsh, Eugene P.; Uhlenbrock, Stefan
 PA USA
 PATENT NO. KIND DATE APPLICATION NO. DATE
 PI US 2003233976 A1 20031225 US 2002-179946 20020625 X
 AB The present invention relates generally to the field of semiconductor integrated circuits and, more particularly, to processes for forming thin films for use in such applications. The present invention provides methods of performing **atomic layer deposition** to form conductive, oxidation-resistant Rh oxide films and films comprising metals, such as Pt, alloyed with Rh oxide. The present invention also provides memory devices and processors comprising films deposited by the above methods.

IT Vapor deposition process
 (chemical, atomic layer; process for direct deposition of atomic layer deposited RhO₂)

IT Films
 (elec. conductive; process for direct **deposition** of atomic layer deposited RhO₂)

IT Electric conductors
 (films; process for direct **deposition** of atomic layer deposited RhO₂)

IT Capacitor electrodes
 Capacitors
 Integrated circuits
 Semiconductor device fabrication
 Semiconductor memory devices
 (process for direct **deposition** of atomic layer deposited RhO₂)

IT Transition metal complexes
 RL: RCT (Reactant); RACT (Reactant or reagent)
 (rhodium, vapor deposition precursor; process for direct deposition of atomic layer deposited RhO₂)

IT 7439-88-5, Iridium, uses 7440-04-2, Osmium, uses 7440-05-3, Palladium, uses 7440-06-4, Platinum, uses
 RL: DEV (Device component use); USES (Uses)
 (conductive layer; process for direct **deposition** of atomic layer deposited RhO₂)

IT 12137-27-8, Rhodium oxide (RhO₂)
 RL: DEV (Device component use); USES (Uses)
 (process for direct **deposition** of atomic layer deposited RhO₂)

IT 10028-15-6, Ozone, processes
 RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (vapor deposition oxidant; process for direct **deposition** of atomic layer deposited RhO₂)

IT 12192-97-1, Dicarbonyl cyclopentadienyl rhodium
 RL: RCT (Reactant); RACT (Reactant or reagent)
 (vapor deposition precursor; process for direct **deposition** of atomic layer deposited RhO₂)

L33 ANSWER 4 OF 7 HCPLUS COPYRIGHT 2004 ACS on STN
 AN 2003:737321 HCPLUS Full-textDN 139:253624
 TI **Atomic layer deposition** methods for layers of aluminum-containing materials
 IN Vaartstra, Brian A.
 PA USA
 PATENT NO. KIND DATE APPLICATION NO. DATE X
 PI US 2003176065 A1 20030918 US 2002-99624 20020314 X
 AB The invention pertains to **atomic layer deposition** methods of Al-containing materials. An Al-containing material deposition method includes depositing a 1st precursor on a substrate in the substantial absence of a 2nd precursor. The 1st precursor can contain a chelate of $\text{Al}(\text{NR}_1\text{R}_2)^x(\text{NR}_3(\text{CH}_2)^z\text{NR}_4\text{R}_5)^y$ or $\text{Al}(\text{NR}_1\text{R}_2)^x(\text{NR}_3(\text{CH}_2)^z\text{OR}_4)^y$; where x is 0, 1, or 2; $y = 3 - x$; z is an integer from 2 to 8; and R_1 to R_5 are independently selected from among hydrocarbon groups containing 1-10 C atoms with Si optionally substituted for at least one C atom. The method includes depositing the 2nd precursor on the 1st deposited precursor, the 2nd precursor containing a N source or an oxidant. A deposition product of the 1st and 2nd precursors includes at least one of an Al nitride or an Al oxide. The deposition method can be **atomic layer deposition** where the 1st and 2nd precursors are chemisorbed or reacted as monolayers. The 1st precursor can further be non-pyrolytic.
 IT Vapor **deposition** process
 (**atomic layer; atomic layer**
 deposition methods for layers of aluminum-containing materials)
 IT Dielectric films
 (**for capacitors; atomic layer**
 deposition methods for layers of aluminum-containing materials)
 IT 7439-88-5, Iridium, uses 7440-06-4, Platinum, uses 7440-16-6,
 Rhodium, uses 7440-21-3, Silicon, uses 7440-32-6, Titanium,
 uses 12033-62-4, Tantalum nitride (Ta_N) 25583-20-4, Titanium nitride
 (Ti_N) 52036-95-0, Titanium boride nitride 403852-89-1, Tantalum
 nitride silicide (Ta_NSi)
 RL: TEM (Technical or engineered material use); USES (Uses)
 (**deposition surface; atomic layer**
 deposition methods for layers of aluminum-containing materials)

L33 ANSWER 5 OF 7 HCPLUS COPYRIGHT 2004 ACS on STN
 AN 2003:717679 HCPLUS Full-textDN 139:222653
 TI Ferroelectric memory device using via etch-stop layer and method for manufacturing same
 IN Song, Yoon-jong; Kim, Ki-nam; Lee, Sang-woo
 PA Samsung Electronics Co., Ltd., S. Korea
 PI PATENT NO. KIND DATE APPLICATION NO. DATE
 US 2003170919 A1 20030911 US 2003-354651 20030129 X
 US 6713310 B2 20040330
 JP 2003273328 A2 20030926 JP 2003-54627 20030228
 PRAI KR 2002-12563 20020308
 KR 2002-65610 20021025
 AB A ferroelec. memory device and a method for manufacturing the same. The ferroelec. memory device comprises a lower interlayer insulating layer formed on a semiconductor substrate. The ferroelec. memory device further comprises at least two adjacent ferroelec. **capacitors** disposed on the lower interlayer insulating layer, an interlayer insulation layer formed over the ferroelec. **capacitors**, leaving a top surface of the ferroelec. **capacitors** exposed, a patterned via etch-stop layer formed on the interlayer insulation layer, leaving the top surface of the **capacitors** exposed, an upper interlayer insulating layer formed on the patterned via etch-stop layer, and a plate line commonly connected to the ≥ 2 adjacent ferroelec. **capacitors**. Thus, integration of the ferroelec. memory device can be substantially increased.
 IC ICM H01L021-00
 NCL 438003000; 257295000
 CC 76-3 (Electric Phenomena)
 IT Vapor deposition process
 (atomic layer deposition; ferroelec. memory device using via etch-stop layer and manufacture of same)
 IT Dielectric films
 Diffusion barrier
 Electric insulators
 Etching
 Ferroelectric capacitors
 Ferroelectric memory devices
 Interconnections, electric
 (ferroelec. memory device using via etch-stop layer and manufacture of same)
 IT 1344-28-1, Alumina, uses 7439-88-5, Iridium, uses 7440-04-2, Osmium, uses 7440-05-3, Palladium, uses 7440-06-4, Platinum, uses 7440-16-6, Rhodium, uses 7440-18-8, Ruthenium, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 11105-01-4, Silicon nitride oxide 12010-77-4, Bismuth titanium oxide (Bi4Ti3O12) 12030-49-8, Iridium oxide (IrO₂) 12033-89-5, Silicon nitride, uses 12036-10-1, Ruthenium oxide (RuO₂) 12047-27-7, Barium titanate (BaTiO₃), uses 12060-59-2, Strontium titanate (SrTiO₃) 12137-27-8, Rhodium oxide (RhO₂) 12626-81-2, Lead titanium zirconium oxide (PbTiO₃-1ZrO₂-103)
 RL: DEV (Device component use); USES (Uses)
 (ferroelec. memory device using via etch-stop layer and manufacture of same)

L33 ANSWER 6 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 2003:628147 HCAPLUS Full-textDN 139:158804
 TI Conformal deposition of noble metal **layers** by **atomic layer deposition** and their application
 IN Aaltonen, Titta; Alen, Petra; Ritala, Mikko; Leskela, Markku
 PA ASM Microchemistry OY, Finland
 PATENT NO. KIND DATE APPLICATION NO. DATE
 PI JP 2003226970 A2 20030815 JP 2003-19678 20030129
 US 2003165615 A1 20030904 US 2002-66315 20020129
 PRAI US 2002-66315 20020129 X
 AB In the process, gaseous noble metal precursors are transported near to substrates in reactors by pulsed charging to form ≤1-layer single mol. layers and then reacted with mol. O(g) whose sources (e.g., H₂O₂) are also pulsed charged into the reactors to afford noble metal layers useful for **capacitor electrodes** of integrated circuits, nonmagnetic interlayers of ultrahigh-d. magnetic disks, etc. The precursors may be metallocenes or β-diketonates. The substrates may be coated with Al₂O₃ or TiO₂ thin films (of thickness 10-20 Å) as seed layers.
 ST **atomic layer deposition** ruthenium
capacitor electrode; ruthenocene sourced ruthenium conformal deposition **ALD**; magnetic disk nonmagnetic interlayer platinum **ALD**
 IT Vapor deposition process
 (atomic layer; conformal deposition of high-quality noble metal **layers** by **atomic layer deposition** using metallocene or diketonate sources)
 IT Capacitor electrodes
 Integrated circuits
 (conformal deposition of high-quality noble metal **layers** by **atomic layer deposition** using metallocene or diketonate sources)
 IT 7439-88-5, Iridium, uses 7440-04-2, Osmium, uses 7440-05-3, Palladium, uses 7440-15-5, Rhenium, uses 7440-16-6, Rhodium, uses 7440-22-4, Silver, uses 7440-57-5, Gold, uses
 RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
 (conformal deposition of high-quality noble metal **layers** by **atomic layer deposition** using metallocene or diketonate sources)
 IT 1287-13-4, Dicyclopentadienylruthenium 7722-84-1, Hydrogen peroxide, processes 7782-44-7, Oxygen, processes 10024-97-2, Nitrogen oxide (N₂O), processes 38625-54-6, Tris(2,2,6,6-tetramethyl-3,5-heptanedionato)ruthenium(III) 94442-22-5, (Trimethyl)methylcyclopentadienylplatinum 250242-94-5, Bis(2,2,6,6-tetramethyl-3,5-heptanedionato)ruthenium(II)
 RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
 (source; conformal deposition of high-quality noble metal **layers** by **atomic layer deposition** using metallocene or diketonate sources)

L33 ANSWER 7 OF 7 HCPLUS COPYRIGHT 2004 ACS on STN
AN 2002:155022 HCPLUS Full-textDN 136:192063
TI Precursor source-material mixture, method for film deposition, and formation of structure
IN Buchanan, Douglas; Neumayer, Deborah Ann
PA International Business Machines Corp., USA
PATENT NO. KIND DATE APPLICATION NO. DATE
PI JP 2002060944 A2 20020228 JP 2001-122174 20010420
PRAI US 2000-553997 20000420
AB A precursor source-material mixture useful for CVD or **ALD** comprises a solution, suspension, or emulsion of an inert liquid containing $M R_1^x R_2^y A_z$, where M = Li, Na, K, Rb, Cs, Fr, Be, Mg, Ti, Zr, Hf, Sc, Y, La, V, Nb, Ta, Cr, Mo, W, Mn, Re, Fe, Ru, Os, CO, **Rh**, Ir, Ni, Pd, Pt, Cu, Ag, Au, Zn, Cd, Hg, B, Al, Ga, In, Tl, Si, Ge, Sn, Pb, As, P, Sb, or Bi, R1, R2 = ligand such as (substituted)alkyl, alkenyl, cycloalkenyl, aryl, alkyne, carbonyl, amide, imide, hydrazide, P compound, nitrosyl, nitryl, nitrate, nitrile, halide, azide, alkoxy, siloxy, or silyl, A = ligand such as phosphine, phosphite, amine, arsine, stibine, ether, sulfide, nitryl, isonitrile, alkene, hydrazine, pyridine, N heterocyclic compound, large cyclic mol., Schiff base, cycloalkene, alc., phosphine oxide, alkylidene, nitrite, alkyne, or H_2O , $x \geq 1$, $x + y =$ valency of M, and $z \geq 0$. A method is also described, for forming a structure such as a wiring structure, a **capacitor**, or a FET using the above mixture
IT **Capacitors**
Field effect transistors
Interconnections, electric
Vapor deposition process
(precursor source-material mixture, method for CVD or **ALD** film deposition, and formation of structure)

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DIALOG(R) File 2:INSPEC

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6937878 INSPEC Abstract Number: B2001-07-2860F-005

Title: Novel electrode barriers for high density ferroelectric nonvolatile memories

Author(s): Desu, S.B.; Vedula, R.; Bhatt, H.D.; Hwang, Y.S.; Zhang, X.

Journal: Physica Status Solidi A vol.184, no.2 p.273-89

Publisher: Wiley-VCH,

Publication Date: 16 April 2001 Country of Publication: Germany

CODEN: PSSABA ISSN: 0031-8965

Abstract: We propose a new electrode-barrier structure for direct integration of lead zirconate titanate (PZT) based **capacitors** onto a polysilicon plug for high density FRAM applications. The electrode-barrier structure is based on noble metal alloys (e.g. Pt-Rh, Pt-Ir, Pt-Ru) and their oxides (e.g. PtRhO_x) which satisfy the needs for an excellent diffusion barrier as well as a high conducting electrode. It has been found that the PtRhO_x/PtRh/PtRhO_x electrode-barrier structure acts as a very good bottom electrode on poly-silicon plug. The bottom PtRhO_x layer has shown excellent diffusion barrier properties for lead, oxygen and silicon up to processing temperatures of 700 degrees C as established by Auger electron spectroscopy and Rutherford backscattering spectroscopy studies. The electrode barriers showed no hillock formation and PZT films deposited on this structure crystallized predominantly in the perovskite phase. The **capacitors** exhibited very good hysteresis properties with remnant polarization (P_r) of 16 μC/cm², a coercive field (E_c) of 32 kV/cm, extremely low fatigue (after 1*10¹⁰ cycles) of 3-4%, imprint (after 3.3*10⁹ cycles) of 8-12%, retention (after 1*10⁵ s) of 2-3% and leakage current density (at 100 kV/cm) less than 10⁻⁸ A/cm². These electrode barriers hold excellent promise for applications in high density FRAM capacitor over bit line (COB) structure.

(26 Refs)

Subfile: B

Descriptors: Auger electron spectra; dielectric hysteresis; dielectric polarisation; diffusion barriers; electrodes; ferroelectric **capacitors**; ferroelectric ceramics; ferroelectric storage; lead compounds; leakage currents; platinum alloys; platinum compounds; rhodium alloys; rhodium compounds; Rutherford backscattering

Identifiers: high density ferroelectric nonvolatile memories; electrode-barrier structure; lead zirconate titanate based **capacitors**; PZT based **capacitors**; polysilicon plug bottom electrode; high density FRAM applications; noble metal alloys; noble metal alloy oxides; diffusion barrier properties; high conducting electrode; PtRhO_x/PtRh/PtRhO_x electrode-barrier structure; Auger electron spectroscopy; Rutherford backscattering spectroscopy studies; perovskite phase crystallized PZT films; hysteresis properties; remnant polarization; coercive field; low fatigue; imprint; retention; leakage current density; high density FRAM capacitor over bit line structure; PZT; Si; PtRhO-PtRh-PtRhO; PbZrO₃TiO₃

Class Codes: B2860F (Ferroelectric devices); B1265D (Memory circuits); B2130 (Capacitors); B2530D (Semiconductor-metal interfaces)

Chemical Indexing:

PtRhO-PtRh-PtRhO int - PtRhO int - PtRh int - Pt int - Rh int - O int - PtRhO ss - Pt ss - Rh ss - O ss - PtRh bin - Pt bin - Rh bin
(Elements - 3,2,3,3)

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DIALOG(R) File 2:INSPEC

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6382773 INSPEC Abstract Number: A1999-23-7780D-001, B1999-12-2810F-002
 Title: Low temperature processed $0.7\text{SrBi}_3/\text{Ta}_2\text{O}_5/\text{TaTiO}_3$ thin films fabricated on multilayer electrode-barrier structure for high-density ferroelectric memories

Author(s): Ryu, S.O.; Joshi, P.C.; Desu, S.B.
 Journal: Applied Physics Letters vol.75, no.14 p.2126-8
 Publisher: AIP,
 Publication Date: 4 Oct. 1999 Country of Publication: USA
 CODEN: APPLAB ISSN: 0003-6951
 Document Number: S0003-6951(99)01240-1
 Abstract: Thin films of solid-solution material $0.7\text{SrBi}_3/\text{Ta}_2\text{O}_5/\text{TaTiO}_3$ ($0.7\text{SBT}-0.3\text{BTT}$) were fabricated on $n/\text{poly} +/\text{-polycrystalline}$ ($n/\text{poly} +/\text{-poly}$) Si substrates by a metalorganic solution deposition technique at a low processing temperature of 650 degrees C using a Pt-Rh/Pt-Rh-O_x structure. The Pt-Rh/Pt-Rh-O_x structure was deposited using an in situ reactive radio frequency sputtering process. The electrodes had a smooth and fine-grained microstructure and were excellent diffusion barriers between the $0.7\text{SBT}-0.3\text{BTT}$ thin film and Si substrate. The ferroelectric ($0.7\text{SBT}-0.3\text{BTT}$) test capacitors using these electrode-barrier grown directly on Si showed good ferroelectric hysteresis properties, measured through $n/\text{poly} +/\text{-poly}$ Si substrate, with $2P_r$ and E_c values of 11.5 $\mu\text{C}/\text{cm}^2$ and 80 kV/cm, respectively, at an applied electric field of 200 kV/cm. The films exhibited good fatigue characteristics (<10% decay) under bipolar stressing up to 10^{11} switching cycles and the leakage current density was lower $10^{-7}\text{A}/\text{cm}^2$ at an applied electric field of 200 kV/cm. The good ferroelectric properties of $0.7\text{SBT}-0.3\text{BTT}$ solid-solution thin films at a low processing temperature of 650 degrees C and excellent electrode-diffusion barrier properties of a Pt-Rh/Pt-Rh-O_x structure are encouraging for the realization of high-density nonvolatile ferroelectric random access memories on silicon substrates. (10 Refs)

Class Codes: A7780D (Ferroelectric domain structure and effects; hysteresis); A7755 (Dielectric thin films); A6855 (Thin film growth, structure, and epitaxy); A8115L (Deposition from liquid phases (melts and solutions)); A6822 (Surface diffusion, segregation and interfacial compound formation); A7780F (Ferroelectric switching phenomena); B2810F (Piezoelectric and ferroelectric materials); B1265D (Memory circuits); B2860F (Ferroelectric devices); B0520J (Deposition from liquid phases)

Chemical Indexing:
 $\text{SrBi}_2\text{Ta}_2\text{O}_9\text{Bi}_3\text{TaTiO}_9$ ss - Bi_2 ss - Bi_3 ss - Ta_2 ss - Bi ss - O_9 ss - Sr ss - Ta ss - Ti ss - O ss (Elements - 5)
 PtRh-PtRhO int - PtRhO int - PtRh int - Pt int - Rh int - O int - PtRhO ss - Pt ss - Rh ss - O ss - PtRh bin - Pt bin - Rh bin (Elements - 2,3,3)

Si sur - Si el (Elements - 1)

Numerical Indexing: temperature 9.23E+02 to 9.73E+02 K

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DIALOG(R) File 2:INSPEC

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6018772 INSPEC Abstract Number: B9810-2860-016

Title: High temperature barrier electrode technology for high density ferroelectric memories with stacked capacitor structure

Author(s): Onishi, S.; Nagata, M.; Mitarai, S.; Ito, Y.; Kudo, J.; Sakiyama, K.; Desu, S.B.; Bhatt, H.D.; Vijay, D.P.; Hwang, Y.

Journal: Journal of the Electrochemical Society vol.145, no.7 p. 2563-8

Publisher: Electrochem. Soc,

Publication Date: July 1998 Country of Publication: USA

CODEN: JESOAN ISSN: 0013-4651

Abstract: This paper describes the novel stacked electrode structure, PtRhO_x/PtRh/PtRhO_x, applicable to stacked memory cells in advanced ferroelectric memories. This structure acts as a stable bottom electrode and a barrier on a polysilicon plug up to 700 degrees C and a stable contact resistance of 1.5 K Omega is obtained at the contact size of 0.6 mu m. In addition to the low leakage current of a lead zirconate titanate [PZT, Pb(Zr_{0.52}Ti_{0.48})O₃] capacitor (10⁻⁸ A/cm² at 3 V), degradation properties of fatigue and imprint are improved compared with conventional Pt electrodes. The decrease of the switched charge is restricted to less than 10% after the fatigue cycle of 10¹¹. These results indicate its promise as a barrier electrode structure for advanced ferroelectric memory integration. (15 Refs)

Subfile: B

Descriptors: contact resistance; ferroelectric capacitors; ferroelectric storage; leakage currents; platinum alloys; platinum compounds; rhodium alloys; rhodium compounds; vacancies (crystal

Identifiers: high density ferroelectric memories; stacked capacitor structure; high temperature barrier electrode; polysilicon plug; contact resistance; leakage current; fatigue cycle; PtRhO_x/PtRh/PtRhO_x; PtRhO-PtRh-PtRhO; PZT; Si; PbZrO₃TiO₃

Class Codes: B2860 (Piezoelectric and ferroelectric devices); B1265D (Memory circuits); B2130 (Capacitors)

Chemical Indexing:

PtRhO-PtRh-PtRhO int - PtRhO int - PtRh int - Pt int - Rh int - O int - PtRhO ss - Pt ss - Rh ss - O ss - PtRh bin - Pt bin - Rh bin
(Elements - 3,2,3,3)

PbZrO₃TiO₃ int - TiO₃ int - ZrO₃ int - O₃ int - Pb int - Ti int - Zr int - O int - PbZrO₃TiO₃ ss - TiO₃ ss - ZrO₃ ss - O₃ ss - Pb ss - Ti ss - Zr ss - O ss (Elements - 4)

Si int - Si el (Elements - 1)

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DIALOG(R) File 2:INSPEC

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5659463 INSPEC Abstract Number: B9709-2860-023

Title: Novel high temperature multilayer electrode-barrier structure for high-density ferroelectric memories

Author(s): Bhatt, H.D.; Desu, S.B.; Vijay, D.P.; Hwang, Y.S.; Zhang, X.; Nagata, M.; Grill, A.

Journal: Applied Physics Letters vol.71, no.5 p.719-21

Publisher: AIP,

Publication Date: 4 Aug. 1997 Country of Publication: USA

CODEN: APPLAB ISSN: 0003-6951

Document Number: S0003-6951(97)00724-9

Abstract: Large scale integration of nonvolatile ferroelectric memories requires reduction in the memory cell size, which dictates the electrode of the capacitor to be in direct electrical contact with the source/drain of the transistor. This has been accomplished in the past using four/five separate electrode- and diffusion-barrier layers. In this letter, we report a novel Pt-Rh-O_{sub x}//Pt-Rh/Pt-Rh-O_{sub x} electrode-barrier structure which acts as an electrode as well as a diffusion barrier for integration of the ferroelectric **capacitors** directly onto silicon deposited using an *in situ* reactive rf sputtering process. The electrodes have a smooth and fine grained microstructure and are excellent diffusion barriers between the PbZr_{0.53}/Ti_{0.47}/O₃ (PZT) and Si substrate and exhibit good thermal stability up to very high processing temperatures of 700 degrees C. The ferroelectric (PZT) test **capacitors** using these electrode barriers grown directly on Si, show well saturated hysteresis loops with P_{sub r} and E_{sub c} of 16 μC/cm² and 30-40 kV/cm, respectively. The **capacitors** exhibit no significant fatigue loss (<5%) up to 10¹¹ cycles and have low leakage currents (2*10⁻⁸ A/cm² at 100 kV/cm). These electrode barriers can be used to directly integrate the thin film **capacitors** on the source/drain of the transistors of the memory cell structure for accomplishing large scale integration. (9 Refs)

Subfile: B

Descriptors: crystal microstructure; dielectric hysteresis; diffusion barriers; DRAM chips; electrodes; elemental semiconductors; ferroelectric **capacitors**; ferroelectric materials; ferroelectric storage; large scale integration; lead compounds; leakage currents; platinum alloys; platinum compounds; rhodium alloys; rhodium compounds; silicon; sputter deposition; thermal stability; thin film **capacitors**

Chemical Indexing:

PbZrO₃TiO₃-PtRhO-PtRh-PtRhO-Si int - PbZrO₃TiO₃ int - PtRhO int - PtRh int - TiO₃ int - ZrO₃ int - O₃ int - Pb int - Pt int - Rh int - Si int - Ti int - Zr int - O int - PbZrO₃TiO₃ ss - PtRhO ss - TiO₃ ss - ZrO₃ ss - O₃ ss - Pb ss - Pt ss - Rh ss - Ti ss - Zr ss - O ss - PtRh bin - Pt bin - Rh bin - Si el (Elements - 4,3,2,3,1,7)

PbZr_{0.53}Ti_{0.47}O₃ int - Ti_{0.47} int - Zr_{0.53} int - O₃ int - Pb int - Ti int - Zr int - O int - PbZr_{0.53}Ti_{0.47}O₃ ss - Ti_{0.47} ss - Zr_{0.53} ss - O₃ ss - Pb ss - Ti ss - Zr ss - O ss (Elements - 4)

Numerical Indexing: temperature 9.73E+02 K

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DIALOG(R) File 2:INSPEC

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5545807 INSPEC Abstract Number: B9705-2860-012

Title: A new high temperature electrode-barrier technology on high density ferroelectric capacitor structure

Author(s): Onishi, S.; Nagata, M.; Mitarai, S.; Ito, Y.; Kudo, J.; Sakiyama, K.; Desu, S.B.; Bhatt, H.D.; Vijay, D.P.; Hwang, Y.

Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No.96CH35961) p.699-702

Publisher: IEEE, New York, NY, USA

Publication Date: 1996 Country of Publication: USA 960 pp.

ISBN: 0 7803 3393 4 Material Identity Number: XX97-00080

Abstract: This paper describes the novel stacked electrode structure, PtRhOx/PtRh/PtRhOx, applicable to stacked memory cells in the advanced ferroelectric memories. This structure acts as a stable bottom electrode on the polysilicon plug up to 700 degrees C, and reduces fatigue of PZT capacitor (less than 10% decrease in remanent polarization up to 10¹⁰/cycle), which indicates its promise as an electrode structure for advanced ferroelectric memory integration. (8 Refs)

Subfile: B

Descriptors: electrodes; ferroelectric **capacitors**; ferroelectric storage

Identifiers: high temperature electrode barrier; ferroelectric capacitor; PtRhOx/PtRh/PtRhOx stacked electrode; ferroelectric memory; bottom electrode; polysilicon plug; fatigue; remanent polarization; 700 C; PZT; PtRhO-PtRh-PtRhO; PbZrO₃TiO₃

Class Codes: B2860 (Piezoelectric and ferroelectric devices); B2130 (Capacitors); B1265D (Memory circuits)

Chemical Indexing:

PbZrO₃TiO₃ ss - TiO₃ ss - ZrO₃ ss - O₃ ss - Pb ss - Ti ss - Zr ss - O ss
(Elements - 4)

PtRhO-PtRh-PtRhO int - PtRhO int - PtRh int - Pt int - Rh int - O int -
PtRhO ss - Pt ss - Rh ss - O ss - PtRh bin - Pt bin - Rh bin
(Elements - 3,2,3,3)

Numerical Indexing: temperature 9.73E+02 K

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